1. A gate-controlled, BIT transit time diode device comprising:

a semiconductor layer in a substrate;

an emitter region in said semiconductor layer;

a barrier region in said semiconductor layer wherein said barrier region is in contact with said emitter region and is laterally adjacent to said emitter region;

a collector region in said semiconductor layer;

a drift region comprising said semiconductor layer between said barrier region and said collector region; and

a gate comprising a conductor layer overlying said drift region, said barrier region, and at least a part of said emitter region with an insulator layer therebetween.

2. The device according to Claim 1 wherein said semiconductor layer comprises one of the group of: n-type doped and p-type doped.

3. The device according to Claim 1 wherein said semiconductor layer comprises silicon.

4. The device according to Claim 1 wherein said semiconductor layer comprises a dopant concentration of less than about 1×10^{15} atoms/cm^3.

5. The device according to Claim 1 further comprising a buried insulator layer underlying said semiconductor layer.

6. The device according to Claim 1 wherein said conductor layer consists of one of the group of: polysilicon, metals, metal silicide, metal nitrides, and combinations thereof.

7. The device according to Claim 1 wherein said insulator layer consists of one of the group of: oxide, silicon oxide, silicon oxynitride, silicon nitride, tantalum oxide, and aluminum oxide.

8. The device according to Claim 1 wherein said emitter region is n-type, said barrier region is p-type, and said collector region is p-type.

9. The device according to Claim 8 wherein said emitter region comprises a dopant concentration of greater than about $1x10^{19}$ atoms/cm^3.

10. The device according to Claim 8 wherein said barrier region comprises a dopant concentration of about $1x10^{18}$ atoms/cm^3.

11. The device according to Claim 1 wherein said emitter region is p-type, said barrier region is n-type, and said collector region is n-type.

12. The device according to Claim 11 wherein said emitter region comprises a dopant concentration of greater than about $1x10^{19}$ atoms/cm^3.

13. The device according to Claim 11 wherein said barrier region comprises a dopant concentration of about $1x10^{18}$ atoms/cm^3.

14. A gate-controlled, BIT transit time diode device comprising:

a substrate;

a buried insulator layer overlying said substrate;

a semiconductor layer overlying said buried insulator layer;

an emitter region in said semiconductor layer;

a barrier region in said semiconductor layer wherein said barrier region is in contact with said emitter region and is laterally adjacent to said emitter region;

a collector region in said semiconductor layer;

a drift region comprising said semiconductor layer between said barrier region and said collector region; and

a gate comprising a polysilicon layer overlying said drift region, said barrier region, and at least a part of said emitter region with an oxide layer therebetween.

15. The device according to Claim 14 wherein said semiconductor layer comprises one of the group of: n-type doped and p-type doped.

16. The device according to Claim 14 wherein said semiconductor layer comprises silicon.

17. The device according to Claim 14 wherein said semiconductor layer comprises a dopant concentration of less than about $1x10^{15}$ atoms/cm^3.

18. The device according to Claim 14 wherein said emitter region is n-type, said barrier region is p-type, and said collector region is p-type.

19. The device according to Claim 18 wherein said emitter region comprises a dopant concentration of greater than about $1x10^{19}$ atoms/cm^3.

20. The device according to Claim 18 wherein said barrier region comprises a dopant concentration of about $1x10^{18}$ atoms/cm^3.

21. The device according to Claim 14 wherein said emitter region is p-type, said barrier region is n-type, and said collector region is n-type.

22. The device according to Claim 21 wherein said emitter region comprises a dopant concentration of greater than about $1x10^{19}$ atoms/cm^3.

23. The device according to Claim 21 wherein said barrier region comprises a dopant concentration of about $1x10^{18}$ atoms/cm^3.

24. A method to form a gate-controlled, BIT transit time diode device in the manufacture of an integrated circuit device comprising:

providing a semiconductor layer in a substrate;

implanting ions into said semiconductor layer to form an emitter region;

implanting ions into said semiconductor layer to form a barrier region;

forming an insulator layer overlying said semiconductor

layer;

depositing a conductor layer overlying said insulator layer;

patterning said conductor layer to form a gate wherein said gate overlies said barrier region and at least a part of said emitter region; and

thereafter implanting ions into said semiconductor layer to form a collector region and to complete said diode device in the manufacture of said integrated circuit device wherein a drift region is formed in said semiconductor layer where said gate overlies said semiconductor layer between said collector region and said barrier region.

25. The method according to Claim 24 wherein said step of implanting ions into said semiconductor layer to form an emitter region comprises arsenic ions, wherein said step of implanting ions into said semiconductor layer to form a barrier region comprises boron ions, and wherein each of said steps are performed using a common masking layer and a common annealing process.

26. The method according to Claim 24 wherein said semiconductor layer comprises silicon.

27. The method according to Claim 24 further comprising forming a buried insulator layer overlying said substrate prior to said step providing a semiconductor layer overlying said substrate.

28. The method according to Claim 24 wherein said semiconductor layer comprises one of the group of: n-type doped and p-type doped.

29. The method according to Claim 24 wherein said said emitter region is n-type, said barrier region is p-type, and said collector region is p-type.

30. The method according to Claim 24 wherein said emitter region is p-type, said barrier region is n-type, and said collector region is n-type.

31. The method according to Claim 24 wherein said conductor layer consists of one of the group of: polysilicon, metals, metal silicide, metal nitrides, and combinations thereof.

32. The method according to Claim 24 wherein said insulator layer consists of one of the group of: oxide, silicon oxide, silicon oxynitride, silicon nitride, tantalum oxide, and aluminum oxide.